L Number	Hits	Search Text	DB	Time stamp
1	2636	dislocation and (doping or implantating)	USPAT; US-PGPUB	2003/05/22 15:07
2	37	(dislocation and (doping or implantating)) and (charge with (accumulation or accumulating or build)	USPAT; US-PGPUB	2003/05/22 15:07
3	3	dislocation and (charge with (accumulation or accumulating or build)	EPO; JPO; DERWENT; IBM_TDB	2003/05/22 14:23
4	112	dislocation and (charge with (accumulation or accumulating or build)	USPAT; US-PGPUB	2003/05/22 15:06
5	75	dislocation and (charge with (accumulation or accumulating or build)) not ((dislocation and (doping or implantation)) and (charge with (accumulation or accumulating or build))	USPAT; US-PGPUB	2003/05/22 14:23
6	73	dislocation and (charge with (accumulation or accumulating or build)) not ((dislocation and (doping or implantation)) and (charge with (accumulation or accumulating or build)) and @ad<=20020222	USPAT; US-PGPUB	2003/05/22 15:07
7	331	dislocation same charge	USPAT; US-PGPUB	2003/05/22 15:31
8	318	dislocation same charge and @ad<=20020222	USPAT; US-PGPUB	2003/05/22 16:40
9	311	(dislocation same charge) and @ad<=20020222 not ((dislocation and doping or implantating) and (charge with (accumulation or accumulating or build)))	USPAT; US-PGPUB	2003/05/22 15:06
10	291	((dislocation same charge) and @ad<=20020222 not ((dislocation and doping or implantating) and (charge with (accumulation or accumulating or build)) not ((dislocation and (charge with (accumulation or accumulating or build))) not ((dislocation and (doping or implantation)) and (charge with (accumulation or accumulating or build))	USPAT; US-PGPUB	2003/05/22 15:08
11	9	(((dislocation same charge and @ad<=20020222) not ((dislocation and doping or implantating) and (charge with (accumulation or accumulating or build)) not ((dislocation and (charge with (accumulation or accumulating or build))) not ((dislocation and (doping or implantation)) and (charge with (accumulation or accumulating or build)) and 438	USPAT; US-PGPUB	2003/05/22 15:10
13	282	(((dislocation same charge and @ad<=20020222) not ((dislocation and doping or implantating) and (charge with (accumulation or accumulating or build))) not ((dislocation and (charge with (accumulation or accumulating or build))) not ((dislocation and (doping or implantation)) and (charge with (accumulation or accumulating or build)))) not ((dislocation same charge) and @ad<=20020222) not ((dislocation and (doping or implantating) and (charge with (accumulation or accumulating or build))) not ((dislocation and (charge with (accumulation or accumulating or build))) not (((dislocation and (doping or implantating)) and (charge with (accumulation or accumulating or build))))) and 438)	USPAT; US-PGPUB	2003/05/22 16:37

14	96	dislocation same charge	EPO; JPO; DERWENT; IBM_TDB	2003/05/22 16:45
18	44	(image with device) same SOI	US-PAT; US-PGPUB	2003/05/22 16:39
19	39	((image with device) same SOI) and @ad<=20020222	US-PAT; US-PGPUB	2003/05/22 16:49
20	19	(((image with device) same SOI) and @ad<=20020222) and MOS	US-PAT; US-PGPUB	2003/05/22 16:44
22	19	(((image with device) same SOI) and @ad<=20020222) and MOS	US-PAT; US-PGPUB	2003/05/22 16:44
23	86	dislocation and (p with n with junction)	EPO; JPO; DERWENT; IBM_TDB	2003/05/22 16:48
24	8	(dislocation and (p with n with junction)) and transistor	EPO; JPO; DERWENT; IBM_TDB	2003/05/22 16:49
25	1023	dislocation and (p with n with junction)	US-PAT; US-PGPUB	2003/05/22 16:49
26	468	(dislocation and (p with n with junction)) and transistor	US-PAT; US-PGPUB	2003/05/22 16:49
27	457	((dislocation and (p with n with junction)) and transistor) and @ad<=20020222	US-PAT; US-PGPUB	2003/05/22 16:49
28	198	(((dislocation and (p with n with junction)) and transistor) and @ad<=20020222) and charge	US-PAT; US-PGPUB	2003/05/22 16:50
29	29	((((dislocation and (p with n with junction)) and transistor) and @ad<=20020222) and charge) and SOI	US-PAT; US-PGPUB	2003/05/22 16:50

ragraph - BSTX (5):
[0003] A second advantage that SOI wafers have over conventional bulk
silicon wafers is the elimination of junction leakage between n-channel and
p-channel devices. Ordinarily, isolated p-channel (for NFETS) and n-channel
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L Number	Hits	Search Text	DB	Time stamp
1	2634	dislocation and (doping or implantating)	USPAT; US-PGPUB	2003/05/22 15:07
2	37	(dislocation and (doping or implantating)) and (charge with (accumulation or accumulating or build))	USPAT; US-PGPUB	2003/05/22 15:07
3	3	dislocation and (charge with (accumulation or accumulating or build	EPO; JPO; DERWENT; IBM_TDB	2003/05/22 14:23
4	114	dislocation and (charge with (accumulation or accumulating or build	USPAT; US-PGPUB	2003/05/22 15:08
5	79	(dislocation and (charge with (accumulation or accumulating or build))) not (dislocation and (doping or implantating) and (charge with (accumulation or accumulating or build)))	USPAT; US-PGPUB	2003/05/22 14:23
6	71	(dislocation and (charge with (accumulation or accumulating or build))) not (dislocation and (doping or implantating) and (charge with (accumulation or accumulating or build)) and @ad<"20020228"	USPAT; US-PGPUB	2003/05/22 15:07
7	331	dislocation same charge	USPAT; US-PGPUB	2003/05/22 15:31
8	318	(dislocation same charge and @ad<"20020228"	USPAT; US-PGPUB	2003/05/22 15:07
9	311	((dislocation same charge and @ad<"20020228") not ((dislocation and (doping or implantating) and (charge with (accumulation or accumulating or build)))	USPAT; US-PGPUB	2003/05/22 15:08
10	297	(((dislocation same charge and @ad<"20020228") not ((dislocation and (doping or implantating) and (charge with (accumulation or accumulating or build)) not (dislocation and (charge with (accumulation or accumulating or build))) not (dislocation and (doping or implantation) and (charge with (accumulation or accumulating or build))	USPAT; US-PGPUB	2003/05/22 15:08
11	9	(((dislocation same charge and @ad<"20020228") not ((dislocation and (doping or implantating) and (charge with (accumulation or accumulating or build)) not (dislocation and (charge with (accumulation or accumulating or build)) not (dislocation and (doping or implantating) and (charge with (accumulation or accumulating or build))) and SOI	USPAT; US-PGPUB	2003/05/22 15:10
13	282	(((dislocation same charge and @ad<"20020228") not ((dislocation and (doping or implantating) and (charge with (accumulation or accumulating or build))) not (dislocation and (charge with (accumulation or accumulating or build))) not (dislocation and (doping or implantation) and (charge with (accumulation or accumulating or build)))) not (((dislocation same charge) and @ad<"20020228") not ((dislocation and (doping or implantating)) and (charge with (accumulation or accumulating or build)))) not (dislocation and (charge with (accumulation or accumulating or build))) not (dislocation and (doping or implantation)) and (charge with (accumulation or accumulating or build))))) and SOI)	USPAT, US-PGPUB	2003/05/22 15:11

14	96	dislocation same charge	EPO; JPO; DERWENT; IBM_TDB 2003/05/22 15:31

US-PAT-NO: 6274894

DOCUMENT-IDENTIFIER: US 6274894 B1

TITLE: Low-bandgap source and drain formation for short-channel
MOS transistors

---------- KWIC ---------

Brief Summary Text - BSTX (22):
Transistors have been previously formed in SiGe epitaxial layers grown on silicon substrates. Such transistors are generally formed by growing a SiGe layer on a silicon substrate, forming a gate conductor over the epitaxial layer, and forming source and drain regions self-aligned to the gate conductor. However, these transistors suffer from limitations associated with having the transistor channel within the SiGe. Because the lattice spacing for SiGe is larger than that for silicon, the SiGe layer either deforms so that the atoms in the SiGe alloy are aligned with those of the underlying silicon (if the SiGe layer is relatively thin), or becomes dislocated, wherein some rows of atoms in the silicon and/or the SiGe are not properly bonded to surrounding atoms (when the SiGe is thicker). Both of these states may be disadvantageous for transistor operation. For example, the lattice deformation by which thin SiGe layers align with an underlying silicon substrate changes the transport properties of the charge carriers which comprise the current along the channel during transistor operation. For p-channel devices, this change in transport properties may increase the transistor drive current and

speed, but for n-channel devices the lattice deformation is believed to cause a degradation of transistor properties. If a SiGe layer is made thick enough that **dislocations** form, on the other hand, transistor performance may be degraded because the **dislocations** act as defects which can increase the resistance of the channel and/or reduce the speed of the device by trapping charge carriers. The above limitations may similarly apply in other cases for which a transistor is formed within a lower-bandgap layer formed on a semiconductor substrate, because most such materials systems also involve materials with mismatched lattice spacings.

Brief Summary Text - BSTX (23):

Use of SiGe in the source/drain regions, but not the channel, of the transistor as recited herein does not share the disadvantages described above. Because the source/drain regions are relatively heavily-doped low-resistance regions, lattice distortion and/or **dislocation** formation have little effect on charge carrier transport in these regions. In fact, the use of SiGe may afford several advantages to the source/drain regions recited herein. SiGe may be doped with boron or phosphorus to levels higher than are possible with pure Si. Higher doping levels allow lower series resistances for SiGe LDD regions, and/or narrower and more effective halo regions. The lower bandgap of SiGe as compared to silicon may also result in lowered contact resistance when SiGe is used at the upper surface of the source or drain region. Similar advantages may be realized with lower-bandgap source/drain materials in other materials systems.

US-PAT-NO: 6028339

DOCUMENT-IDENTIFIER: US 6028339 A

TITLE: Dual work function CMOS device

---------- KWIC ---------

Brief Summary Text - BSTX (9):

This technique also suffers from limitations inherent in the conventional implantation method. Ion implantation may give rise to **dislocations**. The generation of **dislocations** provide paths for leakage of charge out of the wells that store charge in DRAM cells and across junctions. For example, normal VLSI processing conditions usually requires a high dose ion implant, such as the BF.sub.2 ion implant used for p-channel source-drain (S/D) doping (in 0.5 micron technology). This may cause the formation of extended loop **dislocations**. Should **dislocations** occur, the chip fails, therefore, it is desirable to prevent the formation of these **dislocations**.

US-PAT-NO: 5342805

DOCUMENT-IDENTIFIER: US 5342805 A

TITLE: Method of growing a semiconductor material by epilaxy

---------- PWIC ---------

Brief Summary Text - BSTX (4):

These state of the art patented inventions utilize misfit **dislocations** to lower the minority lifetime in semiconductor devices. This can be used to enhance the switching speed of power rectifiers, particularly fast recovery power rectifiers with misfit **dislocations** it becomes possible to obtain localized regions in the device with low minority lifetime close to regions with a high minority lifetime. It also allows for a great amount of freedom to place these misfit **dislocations** in favorable locations. Misfit **dislocations** produce relative small leakage currents and are metallurgically and electrically stable, and thus, device performance does not significantly deteriorate under high power and temperature applications. Unlike processes where misfit **dislocations** had been previously used to remove impurities from the space charge region, in the patented invention, the misfit **dislocations** are used to directly reduce minority carrier lifetime. That becomes possible because they are associated with deep energy levels in the energy gap of silicon, like metallic impurities.

Brief Summary Text - BSTX (15):

It is another object of the present invention to provide an improved semiconductor material and a method for controlling the minority carrier lifetime in regions of devices formed therein in which the misfit **dislocations** are located in a region proximate to or outside a depletion region or outside a space charge region in the case of a forward biased junction.

Detailed Description Text - DETX (19):

If the .tau. in the depletion region is large, IR is small. If .tau. just outside the depletion region is small, the recombination there will diminish the charge in the space charge region when the rectifier is forward biased, which will result in a faster switching time. The misfit **dislocations** in this case must have more regions or more germanium in each 2.mu. region or more gold or/and Pt to achieve the same switching time as in the case of FIG. 1. In some cases only one of the misfit **dislocation** regions might be the preferred embodiment. A similar reasoning is in special cases true for the spare charge region.